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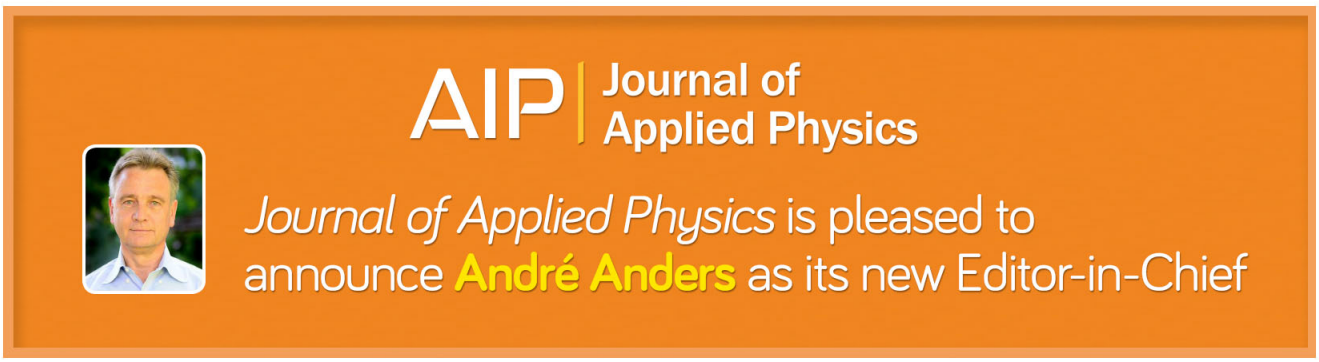

Trap-state density in continuous-wave laser-crystallized single-grainlike silicon transistors

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This investigation characterizes electrical characteristics of continuous-wave green laser-annealed single-grainlike silicon thin-film transistors in relation to trap-state densities. As laser power increases, highly crystalline channels form, reducing tail-state densities to as low as 3×10^{19} eV^{-1} cm^{-3}. This occurrence is responsible for high field-effect electron mobility of 284 cm^2/V s. In contrast, increasing laser power initially reduces the deep-state density and then increases it to 3×10^{16} eV^{-1} cm^{-3}. This reversal in deep-state density and thus in the subthreshold slope as well as a saturating reduction in threshold voltage are associated with the formation of extra interface defects caused by laser-crystallization-enhanced surface roughness. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2209198]

Recently, high-performance polycrystalline silicon thin-film transistors (polysilicon TFTs) on glass substrates have been implemented. They depend on the formation of laser-crystallized single-grainlike channels by sequential lateral solidification (SLS).[1,2] The supply of photoenergy from continuous-wave (cw) green lasers facilitates the lateral crystallization of amorphous silicon (*a*-Si), even in the absence of capping layers and laser power masking.[2] Hence, cw laser crystallization (CLC) is more practical than excimer-laser-annealing (ELA)-based SLS.[1,2]

A high laser power is commonly adopted to enhance the channel crystallinity in an attempt to improve all of the electrical characteristics of laser-crystallized polysilicon TFTs.[3] However, doing so also roughens the channel surfaces while degrading the threshold voltage and the subthreshold slope, as reported by Angelis *et al.* in relation to ELA polysilicon TFTs.[4] A high-speed and reliable transistor should have a thin channel, which fact explains why interfacial properties dominate the performance of transistors. Accordingly, the surface roughness of thin CLC channels is a major concern. Several methods, such as field-effect conductance[5] (FEC) and low-frequency noise methods[6], have been developed and applied to measure channel quality in terms of the density of grain (grain boundary) and interface traps, which effectively specify the electrical parameters of the transistors.[7] Nevertheless, these issues have seldom been addressed for CLC-fabricated TFTs.

This study reveals an ultralow trap-state density in CLC polysilicon, which is consistent with the demonstration of excellent electrical characteristics. Additionally, the formation of extra interface defects induced by the laser-crystallization-enhanced surface roughness (LCESR) leads to the reversal of deep-state density and, thus, the subthreshold slope, as well as a saturating reduction in threshold voltage.

The experiment was begun by sequentially depositing a 50 nm thick layer of SiN_x, a 150 nm thick layer of SiO_2, and a 50 nm thick *a*-Si film by plasma-enhanced chemical vapor deposition (PECVD) on a Corning Eagle 2000 glass substrate. Before laser crystallization, the deposited *a*-Si films were patterned into individual islands of 60 μm/76 μm (width/length) as active layers of TFTs to prevent peeling.[2] A solid-state cw green ($\lambda=532$ nm) laser with an output power of 3–5 W was then guided to crystallize islands laterally by line scanning the samples at 10 cm/s. CLC experiments are conducted in ambient air at room temperature and the laser beam is incident on samples with a strip spot of 220×40 μm^2.

Figures 1(a)–1(c) depict the topographies of *a*-Si channels crystallized by the CLC method at different laser powers. As the laser power increases, CLC, instead of super-lateral-growth (SLG) or even solid-phase crystallization, dominates the growth of the grains.[1,2,8] Consequently, highly crystalline channels comprised micrograins of dimensions 3×10 μm^2 forms. The surface roughness of the channels crystallized with an incremental laser power initially declines from 8.2 nm (3–3.7 W) to 2.8 nm (3.8–4.2 W), before increasing to 5.1 nm (4.3–4.5 W), as indicated by these topographies. The initial decrease in the roughness reflects a change in the crystallization mode because the surface roughness of the SLG-crystallized channels was reported to exceed that of the CLC-crystallized channels.[1,2] The reversal in the roughening of the surface as the laser power is further increased is attributed to the increase in the numbers of hillocks at the grain boundaries, caused by high photoenergy irradiation.[9]

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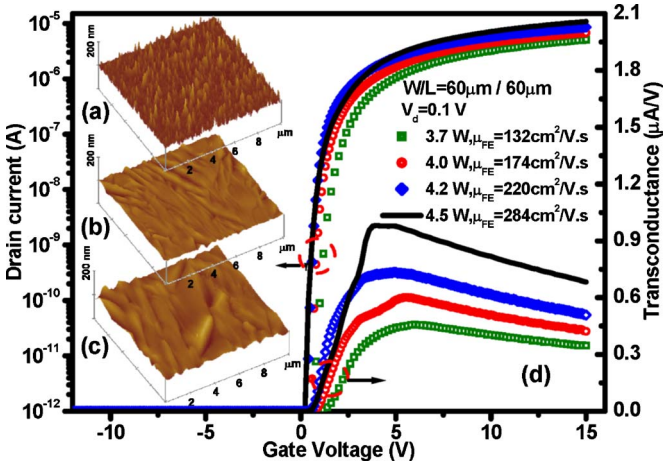

FIG. 1. (Color online) AFM micrographs of channel topographies of polysilicon films crystallized by cw green laser at various laser powers of (a) 3.5, (b) 4.2, and (c) 4.5 W. (d) Transfer characteristics and transconductance curves of polysilicon TFTs made from CLC at laser powers of 3.7, 4.0, 4.2, and 4.5 W.

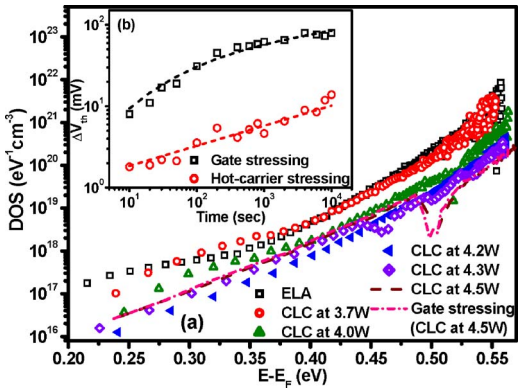

FIG. 3. (Color online) (a) Energy distribution of DOS for polysilicon TFTs made using CLC at laser powers of 3.7, 4.0, 4.2, 4.3, and 4.5 W. For comparison, the DOS distribution for ELA-fabricated TFTs with μ_{FE} of 140 $cm^2/V\,s$, V_{th} of 1.5 V, and S of 180 mV/decade is also presented. (b) ΔV_{th} transients for CLC polysilicon TFTs made at laser power of 4.5 W during gate stressing and hot-carrier stressing. Curve fitting is also shown. The DOS distribution for the same device after gate stressing is also shown in (a).

On various crystallite channels, TFTs are fabricated with conventional polysilicon TFTs. Figure 1(d) plots logarithmic transfer (drain current I_d versus gate voltage V_g) characteristics and linear transcondcutance (G_m) curves for some representative TFTs, when a drain voltage V_d of 0.1 V was applied. Next, the maximum G_m was analyzed to yield the field-effect electron mobility (μ_{FE}), and the threshold voltage (V_{th}) was determined by linear extrapolation of the transcondcutance to zero.[10] The subthreshold slope (S) was also extracted from the maximum slope of the transfer curves, plotted on a semilogarithmic scale. Figure 2 plots the subthreshold slope, the threshold voltage, and the leakage current (at V_d=10 V) against field-effect mobility (laser power).

As expected, increasing the laser fluence increases the efficiency of grain lateral growth, forming larger grains with fewer associated defects, while considerably reducing the height of the barrier to carrier transportation in the channels,

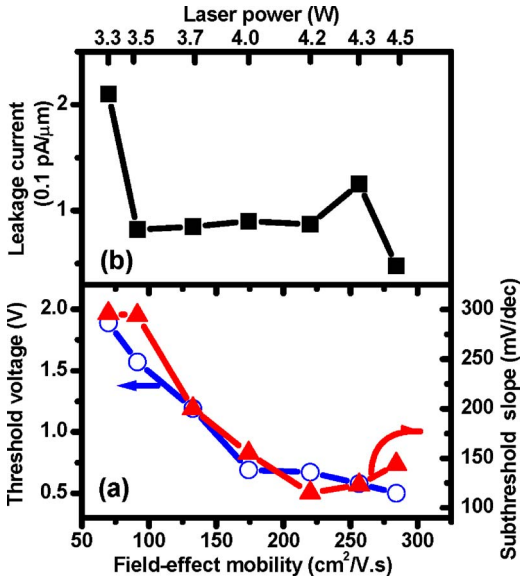

FIG. 2. (Color online) (a) Subthreshold slope and threshold voltage and (b) minimum leakage current for polysilicon TFTs made using CLC at different laser powers in the range of 3–4.5 W.

associated with a higher G_m [Fig. 1(d)], such that μ_{FE} is as plotted in Fig. 2.[11] Next, the densities of states (DOSs) of traps are examined using the FEC method for CLC-fabricated TFTs, with reference to the crystallization conditions, as presented in Fig. 3(a). As the laser power increases to 4.5 W, the tail-state density clearly decreases to 3×10^{19} eV^{-1} cm^{-3} at $E-E_F$=0.52 eV where E_F is the mid-gap energy, whose value is almost one order of magnitude lower than that obtained from ELA-fabricated TFTs [see Fig. 3(a)].[12,13] The enlargement of grains in channels as the laser power increases not only reduces the density of grain defects but also relieves the distortion of bonds in highly crystalline silicon.[13,14] Therefore, channel crystallinity is strongly related to the density of distorted-bond defects, regarded as the origination of tail states. Hence, the tail-state density declines as the laser power increases, as shown in Fig. 3(a), and as indicated by ELA-related results reported elsewhere.[13] Extremely low tail-state densities associated with large grains in CLC polysilicon are responsible for the high μ_{FE} of 284 $cm^2/V\,s$, independently of surface roughness.

Closely examining the four transconductance (G_m) curves in Fig. 1(d) reveals that the slope at which G_m is away from the ascending stage and declines with V_g increases with the laser power. As the surface roughness increases, the mobility reduction at high gate voltages is increased because the surface scattering increases,[14] which relation is consistent with the transconductance data. Note that the electric field enhanced at the rough polysilicon/SiO_2 interface[15] assists the electrons to be injected into the gate oxide.[4] In Fig. 2(a), the threshold voltage decreases more slowly as the laser power increases above 4.0 W, suggesting that the injected electrons are trapped as negative charges in the oxide. The negative trapped charge reduces the electrical field near the drain, reducing the leakage current at high laser power [see Fig. 2(b)].[4]

The charge trapping mechanism can be further investigated by gate stressing[16] and hot-carrier stressing.[17] Figure 3(b) plots the V_{th} shift (ΔV_{th}) versus the stressing time (t) for CLC-fabricated TFTs made at a laser power of 4.5 W during gate stressing (V_g=20 V and V_d=0 V) and hot-carrier stress-

ing (V_g=8 V and V_d=16 V). The former test demonstrates a logarithmic time dependence of ΔV_{th}, which is indicative of charge trapping in gate dielectrics.[16] Moreover, the latter test indicates the power-law time dependence of ΔV_{th} with exponents of 0.25 ($\sim t^{0.25}$), as opposed to power-law exponents in the range of 0.4–0.6 associated with deep-state generation.[17] Comparing DOS distributions before and after either gate stressing [see Fig. 3(a)] or hot-carrier stressing (not shown herein) shows almost overlapping trap-state densities. Hence, slightly roughened CLC polysilicon/SiO_2 merely induces charge trapping but trapped electrons into the gate oxide or at the interface create hardly any new deep states.

Increasing the laser power initially reduces the deep-state densities, unlike the tail-state density, to as low as 1.0×10^{16} $\text{eV}^{-1}\,\text{cm}^{-3}$ at $E-E_F$=0.25 eV and then increases these to 3×10^{16} $\text{eV}^{-1}\,\text{cm}^{-3}$. Deep-state densities extracted at other energetic states of $E-E_F$=0.25–0.35 eV also exhibit the same trend. Low-frequency noise measurements indicate that roughened surfaces formed extra interface traps,[4,6,7] which are responsible for the reversal in the deep-state density.[18] For ELA polysilicon, the impact of LCESR on the deep-state density is difficult to observe because in such a material, the deep-state density is as high as 5×10^{17} $\text{eV}^{-1}\,\text{cm}^{-3}$ (at $E-E_F$=0.25 eV), exceeding that of polysilicon-oxide traps, 3×10^{17} $\text{eV}^{-1}\,\text{cm}^{-3}$.[4,12] The deep-state density of smooth and single-grainlike CLC polysilicon is below 10^{17} $\text{eV}^{-1}\,\text{cm}^{-3}$, causing LCESR to change the deep-states to reverse the decline, despite the fact that increasing channel crystallinity normally reduces the density of the grain defects, including deep-states defects. Therefore, the deep-state- and/or the interface-state-dominated subthreshold slopes follow the variation in deep-states densities with laser power [see Figs. 2(a) and 3(a)].[19,20]

In summary, the measurement of the trap-state densities of CLC polysilicon TFTs was reported to characterize the electrical parameters of devices with reference to channel crystal quality and surface morphology. Ultralow trap-state densities associated with smooth and single-grainlike polysilicon are responsible for higher field-effect mobility, lower threshold voltage, steeper subthreshold slope, and lower leakage current than those of ELA-fabricated TFTs. Moreover, low deep-state densities remain sensitive to the interfacial states and are influenced by the LCESR effect.

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